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(54) Method of forming an SOI structure with a DRAM

Verfahren zur Herstellung einer SOI-Struktur mit einem DRAM

Procédé de fabrication d'une structure du type SOI avec DRAM

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Description

The present invention concerns a method of forming an SOI structure and a semiconductor memory device. SOI has been used as a structure for electronic parts such as semiconductor devices and the present invention can be utilized as a method of forming various kinds of SOI structures.

More specifically, it can be used, for example, to SRAM or EEPROM. In EEPROM, it relates, in particular, to a method of manufacturing a non-volatile memory device in which a control gate electrode layer is laminated by way of an insulator film on a floating gate electrode layer.

Description of the Prior Art

The SOI (silicon on insulator) structure has been utilized mainly in the field of electronic materials by a method of forming various kinds of semiconductor devices to a silicon portion disposed on an insulator layer.

As one of means for forming the SOI structure, it has been known a technique for bonding a substrate to another silicon substrate formed with an insulator portion on the side of the insulator portion and polishing the silicon substrate thereby providing a structure in which the silicon portion is present on the insulator portion. It is generally referred to as a bonded SOI or the like.

Since the bonded polished type SOI structure and a process therefor enables high integration of electronic materials and makes it possible to assemble devices above and below the silicon portion, it contributes to increase of the integration degree of IC or the like.

Description will now be made to a method of forming the bonded SOI structure with reference to Fig. 1-A to Fig. 1-G (refer to M. Hashimoto et. al. "Low Leakage SOIMOSFETs Fabricated Using a Wafer Bonding Method" in Extended Abstracts of the 21st Conference on Solid State Devices and Material 15, Tokyo, 1989, pp. 89 - 92 n).

As shown in Fig. 1-A, one surface of a silicon substrate 1 (highly flattened silicon wafer is generally used and referred to as a substrate A) is patterned by using photolithography or etching technology to form a recess at a depth of 1500 Å (10 Å = 1 nm) or smaller.

Then, an insulator portion 2 is formed by forming an SiO_2 film on the surface by means of CVD or the like. Thus, a structure in which the insulator portion 2 is formed on one side of the silicon substrate 1 is obtained as shown in Fig. 1-B. The insulator portion 2 is formed as a film having unevenness as illustrated in the figure in accordance with the surface shape of the patterned silicon substrate 1.

Further, a polysilicon film 3 is formed to a thickness of about 5 um on the insulator portion 2, for example, by CVD. Thus the structure shown in Fig, 1-C is obtained. The polysilicon film 3 is provided for forming a highly smooth bonding surface upon bonding a separate substrate 4 (substrate 4 shown in B in Fig. 1-E) in the subsequent step.

Then, the surface of the polysilicon film 3 is polished to flatten, to attain a highly smooth surface. In this case, the thickness of the polysilicon film 3 as a remaining film is made to a thickness of 3 um or less.

Another substrate 4 (hereinafter referred to as substrate B) is brought into a close contact with the polished surface of the polysilicon film 3. Both of the surfaces are joined in close pressure bonding to obtain a joined structure as shown in Fig. 1-E. It is generally said that firm joining is attained due to hydrogen bonds present between both of the surfaces. Usually, they are thermally joined by heating to attain an extremely firm bonding. The bonding strength is generally greater than 200 kg/cm^2 and, sometimes, reaches as great as 2000 kg/cm^2, As another substrate 4 (substrate B) to be bonded, the same silicon substrate as the substrate 1 (substrate A) is usually employed, because a failure may be caused unless physical property such as thermal expansion coefficient is equal between them since they are often put to a heating step subsequent to the bonding. If there is no such problem, another substrate 4 is not necessarily a silicon substrate since this functions only as a support bed in the prior art, for example, shown in the drawing. However, in a case of forming a device also on the another substrate 4 (substrate B) to be appended, it has to be a semiconductor substrate capable of forming a device.

Then, the substrate 1 is ground so as to leave a silicon portion of the substrate 1 to about 5 um or less as the remaining film to attain a structure shown in Fig. 1-F. Fig. 1-F is turned from state in Fig. 1-E, because the structure is turned upside to down to situate the substrate 1 above for this grinding or for the subsequent selective polishing.

Then, selective polishing is applied. In this case, polishing of precious finishing is applied till the insulator portion 2 is just exposed. This provides a structure as shown in Fig. 1-G in which a silicon portion 10 is present on the insulator portion 2 being surrounded with undulating insulator portion 2. The silicon portion 10 forms a SOI film. To a structure in which the silicon portion 10 is present on the insulator portion 2 (SOI structure), various kinds of devices are formed to the silicon portion 10 (SOI film). As shown in Fig. 1-G, since each of the silicon portions 10 is surrounded with the insulator portion 2, a structure in which device isolation is attained from the first is provided.

Further, in a method of manufacturing the SOI substrate as described above, since the film thickness 10 in Fig. 1-G varies within a wafer surface, the thickness of an inland single crystal silicon thin film formed to or required pattern also varies.

Further, selective polishing is applied till the boundary between the silicon wafer and the silicon oxide film is exposed in order to obtain a required pattern for the single crystal silicon thin film. In this case, since an over

polishing is required to some extent, the surface of silicon is exposed to an alkaline polishing solution for a long period of time, to roughen the silicon surface. If a TFT (thin film transistor) is formed on the roughened silicon surface, a device with good characteristics can not be obtained since the reliability of a gate insulator film is lowered.

Further, in the SOI process utilizing the bonding polishing method as described above or an electrostatic pressure bonding method, since various kinds of devices can be assembled to the surface and the rear face of the SOI portion (the silicon portion 10 in Fig. 1-G), the mounting density can be increased. By adopting this technology, the size of a memory cell, for example, DRAM can be reduced. However, although the density of a circuit such as a memory cell has been intended to increase in the prior art, the merit of this technique is not effectively utilized for peripheral circuits. For instance, referring to a memory device such as a DRAM or SRAM, although it has been considered to reduce the size of the memory cell by using the SOI technology, the SOI technology is not always utilized for other peripheral circuits and, for example, it has not been conducted to increase the density for the transistor as the peripheral circuit, thereby improving the performance (for example, increasing the operation speed).

Further, for the method of forming a memory device such as EEROM, electric characteristics can be improved outstandingly by applying the polishing method used for SOI.

That is, as shown in Fig. 2, when a floating gate electrode layer is formed, the surface is not flattened but pointed protrusions 15 are formed. Then, an electric field is concentrated to a portion where the protrusions 15 are present in this structure.

Accordingly, in a second gate insulator film between the floating gate electrode 13 and the control gate electrode 14, there is a portion where the thickness is decreased by the protrusions 15. If LSI is manufactured in such a state and applied with a voltage, the electric field is concentrated to a portion where the protrusions 15 are present. Then, electrons in the floating gate electrode are extracted by the electric field applied to the control gate electrode due to the concentration of the electric field, to result in signal data possessing characteristic, thereby bringing about a problem incapable of maintaining the threshold value of a memory transistor at a high level.

It is an object of the present invention is to attain mounting at a further increased density by using the SOI technique and provide a method of forming a SOI structure that effectively utilizes the merit of the SOI technique, also in peripheral circuits as outlined in the claim.

Fig. 1-A through Fig. 1-G show a conventional method of manufacturing bonding type SOI;

Fig. 2 shows a structural view of a conventional EEPROM;

Fig. 3-A through Fig. 3-F show a process for producing a semiconductor device of a SOI structure as an example according to the present invention;

Fig. 4-A through Fig. 4-F show a process for producing a semiconductor device of a SOI structure as a further example.

Descriptions will now be made to an example according to the present invention with reference to Fig. 3-A through Fig. 3-F.

As shown in Fig. 3-A, one of the surfaces of a silicon substrate 31 is patterned.

Then, an insulator portion 32 is formed and the first conductive portions 43a, 43b (a first gate electrode in this example) are formed at one position on the surface of the silicon substrate 31 formed with the insulator portion 32, that is, at a position to form a transistor as a peripheral circuit in this example, to provide a structure as shown in Fig. 3-B.

Then, a connection hole 44 is formed to define a filled connection portion 45 at the other position on the same surface of the silicon substrate 31, that is, at a position to form a cell portion of a semiconductor memory device such as DRAM in this example to provide a structure as shown in Fig. 3-C.

Then, a groove 46 is formed on the connection portion 45 and a trench function portion (a memory capacitor comprising a storage electrode 47 and a capacitor insulator film 48 in this illustrated example) is formed to provide a structure shown in Fig. 3-D.

Subsequently, a polysilicon film 33 is properly formed and polished (refer to Fig. 3-E) and with another substrate 52 is bonded. Although the substrate 52 is not particularly illustrated in Fig. 3, it is the same as that in the case of Fig. 1.

Further, the silicon substrate 31 is polished on the surface of the other side to form a silicon portion 40 and, subsequently, a second electroconductive portion (second gate electrodes 49a, 49b of the transistor on the side of the peripheral circuit and the second gate electrode 49c on the side of the cell as the word electrode) is formed on one and the other positions to form a SOI structure as shown in Fig. 3-F.

Specifically, this example comprises steps (1) - (7) described below as actual constitutions.

The process for the steps is shown successively.

(1) Silicon RIE is applied for forming inter-device isolation regions to the silicon substrate 31. The etching depth is set to about 100 nm or less. Thus, a structure shown in Fig. 3-A is obtained.

(2) An insulator portion 32 comprising SiO_2 is formed by surface oxidation. This also serves as a first gate insulator film 41 of the transistor in the peripheral circuit. Further, a first gate electrode as the first conduction portion 43a, 43b is formed with polysilicon or the like.

(3) An inter-layer film 50 is formed over the entire

surface, for example, by CVDSiO_2. A contact as a connection hole 44 is perforated for leading out a storage electrode in the cell portion and filled with polysilicon to form a connection portion 45 (polysilicon plug). This can be obtained by entirely forming polysilicon and then etching back it. A structure shown in Fig. 3-C is thus obtained.

(4) Further, after depositing SiO_2 as an inter-layer film 51 by a CVD process, a groove 46 is formed to the cell portion as a groove for forming the storage electrode. After perforating the groove 46, polysilicon or the like is formed over the entire surface (refer to a portion shown by the dotted line in Fig. 3-D) and, subsequently, etched back to form a storage electrode 47.

(5) A capacitor insulator film 48 is formed by using a silicon nitride film or the like. A structure shown in Fig. 3-D is obtained.

(6) Then, a plate electrode 33 is formed, for example, with polysilicon and the surface is flattened by grinding. A structure as shown in 1-E is thus obtained.

(7) Polished surfaces of the support substrate 52 (not illustrated) and the plate electrode 33 are adhered by a bonding or electrostatic press bonding process to conduct bonding. Then, the silicon substrate 31 on the side of the device is ground using SiO_2 as the insulator portion 32 as a stopper. Further, the surface is oxidized to form a SiO_2 film 42. Second conduction portions 49a, 49b, 49c are formed, for example, with polysilicon thereover to form a gate electrode. This constitute a word line (second conduction portion 49c) in the cell, and a second electrode (second conductive portions 49a, 49b) of the double gate in the peripheral circuit. The second electrode is previously connected with the first electrode by means of a contact hole.

Subsequently, by way of the same steps as those of various kinds of steps employed so far for forming the memory cell and the peripheral circuit thereof (source, drain injection or formation of aluminum wires), to form a semiconductor memory device.

According to this example, since the peripheral transistor circuit can also be constituted with the double gate, high speed performance of the peripheral circuit can also be realized.

Description will then be made to a further example.

Fig. 4 shows a process flow of this example. The method of forming the SOI structure in this example, comprises forming an insulator portion 62 on one side of a silicon substrate as shown in Fig. 4-B, bonding another substrate 80 on the side thereof formed with the insulator portion 62 (bonding on the upper surface in Fig. 4-E), and polishing the other side of the silicon substrate 61, thereby obtaining an SOI structure in which a silicon portion 70 is present on the insulator layer 62 as shown in Fig. 4-F. The method comprises each of the following steps.

One of the surfaces of the silicon substrate is patterned as shown in Fig. 4-A.

Then, the insulator portion 62 is formed on the patterned surface and, further, openings 66a, 66b at the positions on one side of the surface of the silicon substrate 61 formed with the insulator layer 62, that is, at the position to form a transistor as the peripheral circuit in this example, while a connection hole 75 is formed at the other position on the same surface of the silicon substrate 61, that is, at the position to form a cell portion of a semiconductor memory device such as DRAM in this example to attain a structure as shown in Fig. 4-D.

Then, the openings 66a, 66b are filled with polysilicon or the like to form first conduction portions 72a, 72b, that is, the conduction portions 72a, 72b as the first gate electrode of the peripheral transistor in this example. At the same time, the connection hole 75 is filled to form a connection portion 76 to attain a structure as shown in Fig. 4-C.

Then, a groove 77 is formed on the connection portion 76 and a trench function portion (same memory trench capacitor as in Example 2) to the groove 71 to attain a structure as shown in Fig. 4-D.

Subsequently, by way of the structure shown in Fig. 4-E in the same manner as in the method of Figs 3A-3F, another substrate (not illustrated) is bonded, the other surface of the silicon substrate 61 is polished to form a silicon portion 70 and then the same second conduction portions 74a - 74c as in Example 1 are formed at one and the other positions to attain a SOI structure as shown in Fig. 4-F.

The method of forming the first conduction portions 72a, 72b (first electrode) in this example is different from that of Figs. 3A-3F in which the conduction material (polysilicon) upon forming the polysilicon plug in the cell portion as the connection portion 76 is used also as the double gate first electrode of the peripheral transistor. The first gate oxide film 71 in the peripheral circuit is removed by etching using a diluted fluoric acid in the cell portion by using a resist mask in the step before Fig.4-B to attain a structure as shown in Fig. 4-B. The subsequent steps are the same as those of Figs. 3A-3F.

The insulator portion 62 can be formed by applying CVD to SiO_2. Further, 68 in Fig. 4 denotes an inter-layer film which in formed from SiO_2 by CVD or the like.

This example can also provide the same effect as that in the method of Figs. 3A-3F.

In the method of Figs. 3 and 4 the first conduction portion is formed as the first electrode for constituting the double gate of the peripheral transistor of the memory device but the present invention is not restricted only thereto.

As has been described above according to the present invention, further increased density can be attained by using the SOI technique.

Claims

1. A method of forming a DRAM having a memory cell area and a peripheral transistor area, said memory cell area comprising a trench capacitor, said method comprising the following steps:

   patterning one of the surfaces of a silicon substrate (31) and forming a first gate insulator (32) therein,
   forming a first gate electrode (43a,43b) on the gate insulator at the peripheral transistor area,
   forming a first insulating layer (50) over said one of the surfaces of the silicon substrate (31),
   forming a connection hole (44) in said first insulating layer (50) at the memory cell area and filling a conductive material (45) into the connection hole,
   forming a second insulating layer (51) over said first insulating layer (50),
   forming a groove (46) in the second insulating layer and forming a trench capacitor function portion (47,48) to the groove wherein the trench capacitor function portion is connected to the conductive material in the connection hole,
   bonding another substrate over the second insulating layer, on which the trench capacitor is formed,
   polishing the other surface of said silicon substrate (31) to form a first silicon portion at the peripheral transistor area and a second silicon portion at the memory cell area,
   forming a second gate electrode (49a,49b) over the first silicon portion which functions as double-gate transistor with the first gate electrode, and
   forming a third gate electrode (49c) over the second silicon portion which is connected with the trench capacitor.

Patentansprüche

1. Verfahren zur Herstellung eines DRAM mit einem Speicherzellenbereich und einem peripheren Transistorbereich, wobei der Speicherzellenbereich einen Grabenkondensator aufweist und das Verfahren die folgenden Schritte aufweist:

   Strukturieren einer der Oberflächen eines Siliziumsubstrats (31) und Ausbilden eines ersten Gateisolators (32) darin,
   Ausbilden einer ersten Gateelektrode (43a, 43b) auf dem Gateisolator in dem peripheren Transistorbereich,
   Ausbilden einer ersten Isolationsschicht (50) über der einen der Oberflächen des Siliziumsubstrats (31),
   Ausbilden eines Verbindungslochs (44) in der ersten Isolationsschicht (50) in dem Speicherzellenbereich und Einfüllen eines leitfähigen Materials (45) in das Verbindungsloch,
   Ausbilden einer zweiten Isolationsschicht (51) über der ersten Isolationsschicht (50),
   Ausbilden eines Vertiefung (46) in der zweiten Isolationsschicht und Ausbilden eines Grabenkondensator-Funktionsabschnitts (47, 48) in der Vertiefung, wobei der Grabenkondensator-Funktionsabschnitt mit dem leitfähigen Material in dem Verbindungsloch verbunden wird,
   Bonden eines anderen Substrats über die zweite Isolationsschicht, auf welcher der Grabenkondensator gebildet ist,
   Polieren der anderen Oberfläche des Siliziumsubstrats (31), um einen ersten Siliziumabschnitt in dem peripheren Transistorbereich und einen zweiten Siliziumabschnitt in dem Speicherzellenbereich zu bilden,
   Ausbilden einer zweiten Gateelektrode (49a, 49b) über dem ersten Siliziumabschnitt, welche mit der ersten Gateelektrode als Doppelgate-Transistor funktioniert, und
   Ausbilden einer dritten Gateelektrode (49c) über dem zweiten Siliziumabschnitt, welcher mit dem Grabenkondensator verbunden ist.

Revendications

1. Procédé de formation d'une DRAM possédant une région de cellule de mémoire et une région de transistor périphérique, ladite région de cellule de mémoire comportant un condensateur en tranchée, ledit procédé comportant les étapes suivantes :

   configuration de l'une des surfaces d'un substrat de silicium (31) et formation d'un premier isolant de grille (32) dans celle-ci,
   formation d'une première électrode de grille (43a, 43b) sur l'isolant de grille dans la région du transistor périphérique,
   formation d'une première couche isolante (50) sur ladite première des surfaces du substrat de silicium (31),
   formation d'un trou de connexion (44) dans ladite première couche isolante (50) dans la région de cellule de mémoire et remplissage d'un matériau conducteur (45) dans le trou de connexion,
   formation d'une seconde couche isolante (51) sur ladite première couche isolante (50),
   formation d'une gorge (46) dans la seconde couche isolante et formation d'une partie de condensateur en tranchée (47, 48) dans la gorge, la partie de condensateur en tranchée étant reliée au matériau conducteur dans le trou de

connexion,
liaison d'un autre substrat au-dessus de la seconde couche isolante, sur laquelle est formé le condensateur en tranchée,
polissage de l'autre surface dudit substrat de silicium (31) pour former une première partie de silicium dans la région du transistor périphérique et une seconde partie de silicium dans la région de cellule de mémoire,
formation d'une seconde électrode de grille (49a, 49b) au-dessus de la première partie de silicium qui fonctionne en tant que transistor à double grille avec la première électrode de grille,
formation d'une troisième électrode de grille (49c) au-dessus de la seconde partie de silicium qui est reliée au condensateur en tranchée.

Fig.1(A)

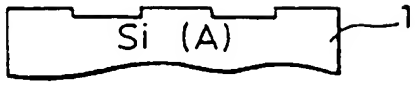


Fig.1(B)

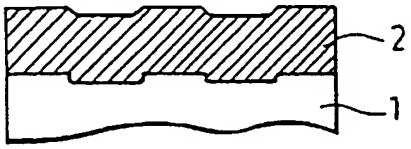


Fig.1(C)

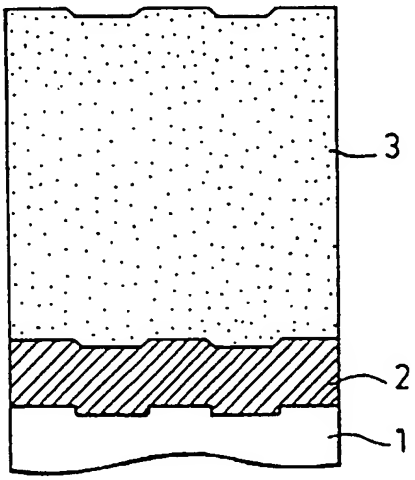
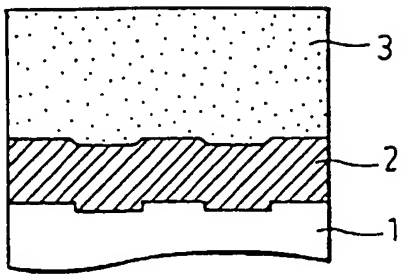


Fig.1(D)



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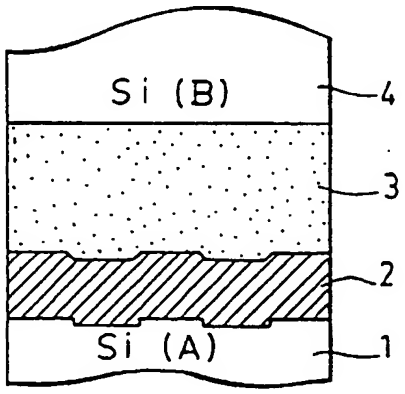

Fig.1(F)

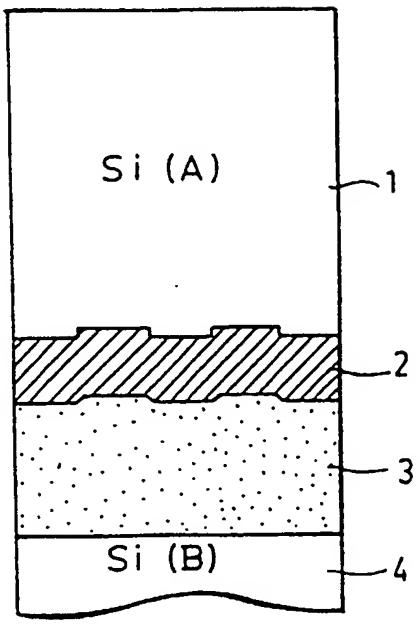

Fig.1(G)

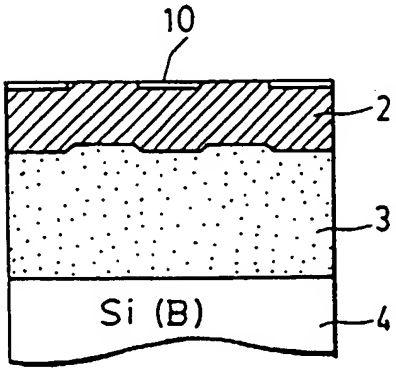

Fig.2

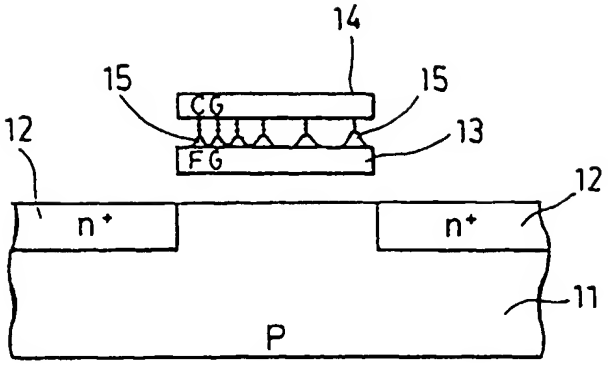

Fig.3(A)

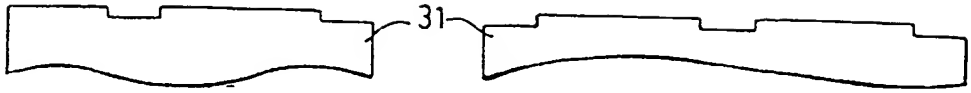

Fig.3(B)

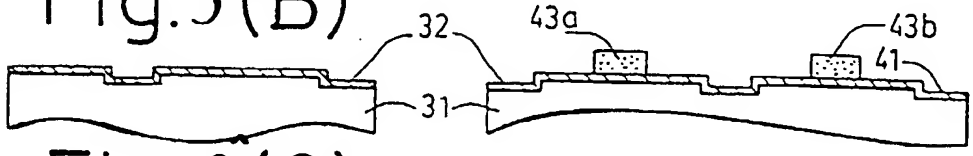

Fig.3(C)

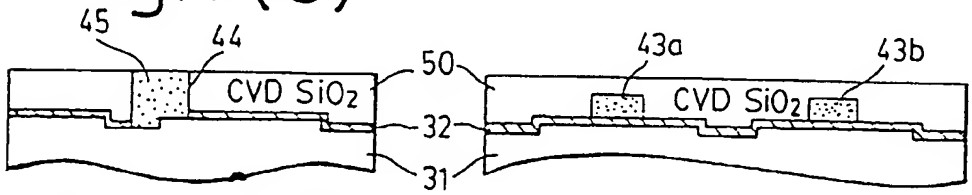

Fig.3(D)

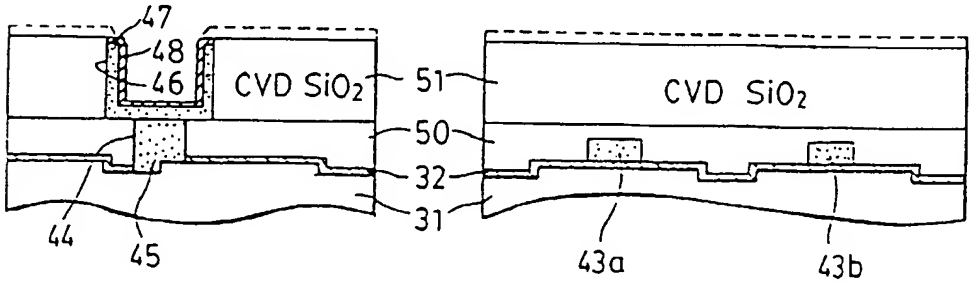

Fig.3(E)

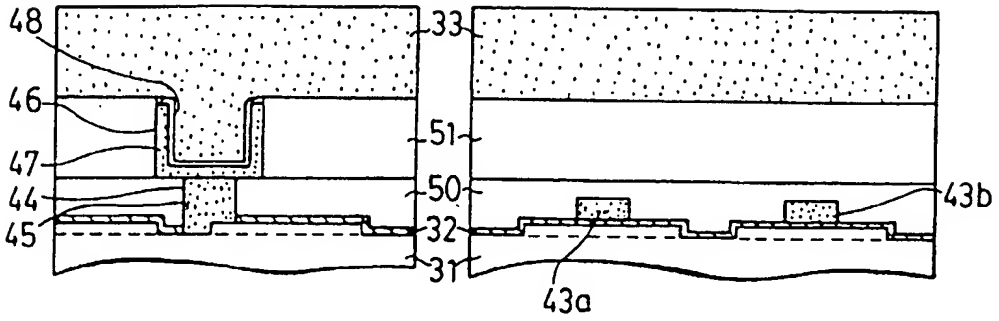
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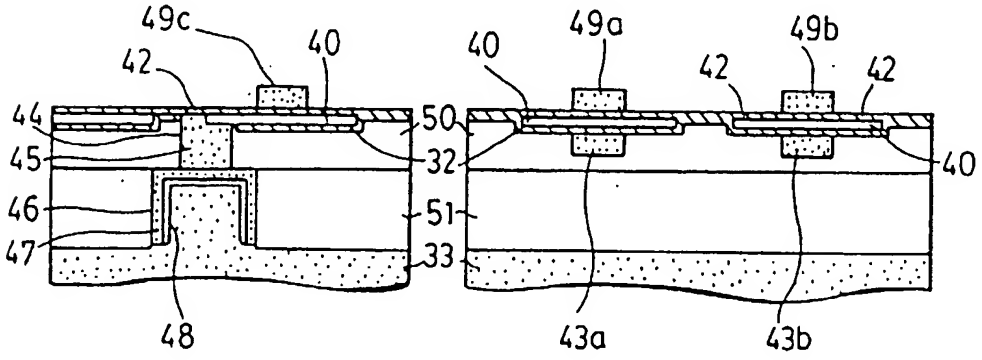
Fig.3(F)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49a
42
49b
42
40
43a
43b

Fig.4(A)

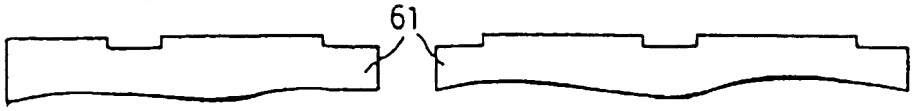


Fig.4(B)

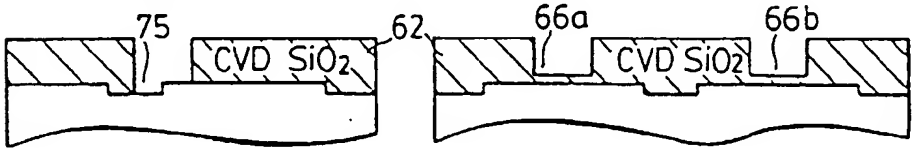


Fig.4(C)

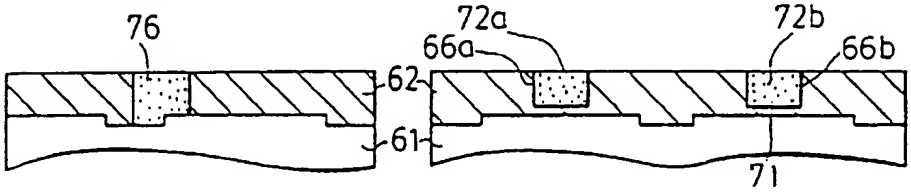


Fig.4(D)

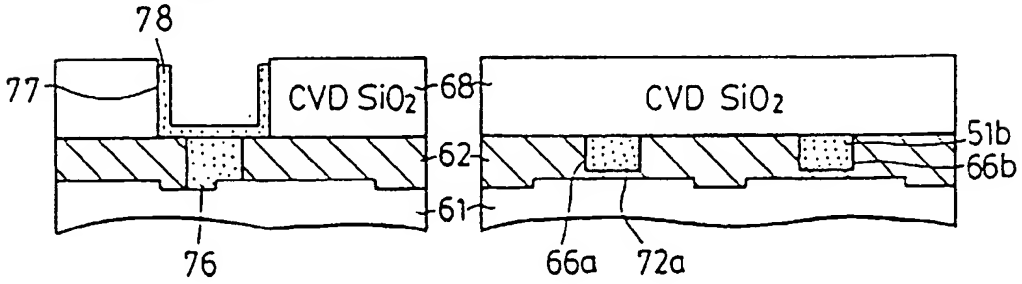


Fig.4(E)

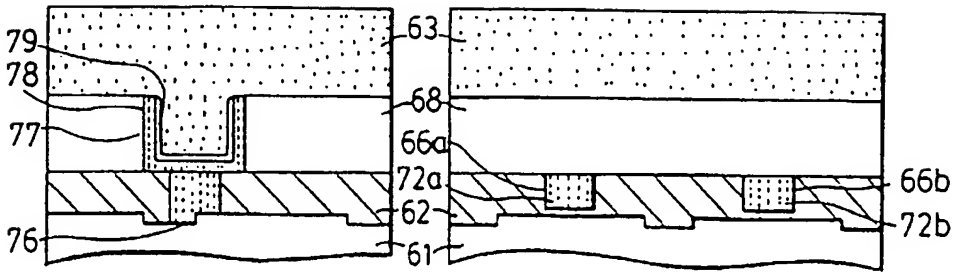
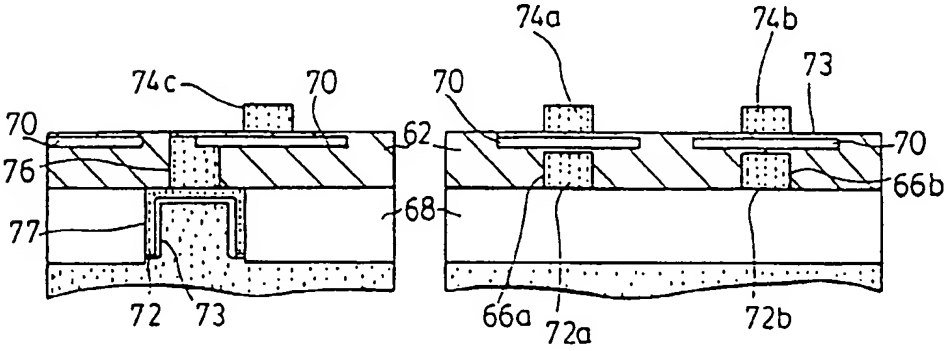

79
78
77
76
63
68
66a
72a
62
61
66b
72b

Fig.4(F)


74c
70
70
76
77
72
73
62
68
74a
74b
73
70
66b
66a
72a
72b